

Printed Circuit Board modeling based on a Cauwer Ladder Network approach combined with GaN Transistors

W. Chen¹, T. Henneron¹, L. Pace², S. Clénet¹ and H. Taha¹

¹Univ. Lille, Arts et Métiers Institute of Technology, Centrale Lille, Junia, ULR 2697 - L2EP, F-59000 Lille, France

²Ecole Centrale de Lyon, INSA Lyon, Univ. Claude Bernard Lyon 1, CNRS, Ampère, UMR5005, 69130 Ecully, France

To design efficient power converter, the electromagnetic behavior of the printed circuit board (PCB) at high switching frequencies should be well-known. Then, numerical approaches can be investigated to analyse the voltage and current waveforms as well as the current density distribution associated with a PCB layout. In this communication, considering a half-bridge converter connected to a passive electrical load, we propose a co-simulation based on the Cauwer Ladder Network (CLN) approach providing an equivalent circuit of the PCB combined with models of GaN transistor and passive components.

Index Terms—CLN approach, co-simulation, GaN transistor, PCB.

I. INTRODUCTION

DUE to the development of semi-conductors used in power converters, switching frequencies have significantly increased. Then, the influence of the electromagnetic behavior associated with the PCB cannot be neglected with regard to power switches and passive components during the design phase of a converter. To study the behavior of a PCB layout, numerical approaches can be investigated. In the literature, the Partial Element Equivalent Circuit (PEEC) modelling method is commonly used to determine a differential equation system based on global electrical quantities (currents and electric potentials) [1]. The PEEC approach does not require a mesh of the air surrounding the conductive tracks but a dense matrix system needs to be solved. Another approach is to apply the Cauwer Ladder Network (CLN) approach to the magneto-quasistatic Finite Element (FE) model of a PCB in order to define an equivalent circuit composed of resistors and inductances [2]. The CLN approach facilitates easy coupling with equivalent circuit models of other components and enables the calculation of field distributions (current density, magnetic field, ...).

In this communication, based on a half-bridge converter supplying a passive electrical load, the equivalent CLN circuit of the PCB is combined with models of GaN transistor to perform a co-simulation. In a first part, the studied system is introduced. The second part presents the model of the PCB obtained when applying the CLN approach. In a third part, a co-simulation based on the equivalent CLN circuit of the PCB combined with PSICE models of GaN transistor is done.

II. STUDIED DEVICE

The studied system is based on a half-bridge converter supplying an electrical load composed of a resistor R_c and of an inductance L_c (Fig. 1). The converter is composed of two GaN transistors, K_1 and K_2 , and of two capacitors, C_1 and C_2 , connected to the PCB. The switching frequency is fixed to $f = 1$ MHz, the duty cycle to 0.5 and the voltage U of the DC bus to 180 V.

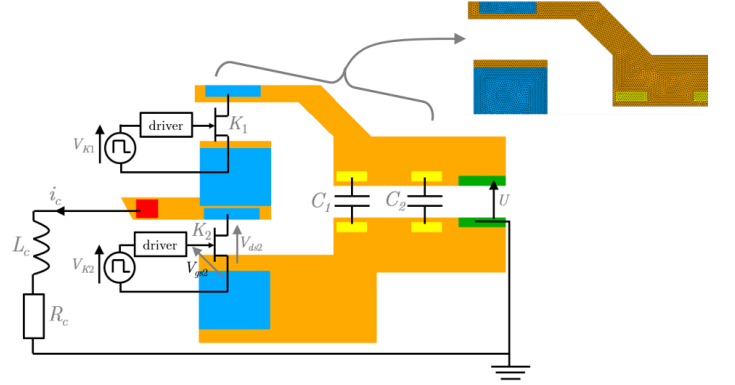


Fig. 1. Studied device and part of the PCB mesh.

III. NUMERICAL MODEL OF THE PCB BASED ON THE CLN APPROACH

To take into account the resistive and inductive effects of the PCB, a magneto-quasistatic problem is considered. The PCB, excluding the conductive tracks connected to the transistor gates, forms a conductive subdomain D_c . The studied domain D is composed of the subdomain D_c enclosed within an air box. To solve the problem, a FE model based on the $\mathbf{A} - v$ formulation is used where $\mathbf{A}$ is the magnetic vector potential and v the electric scalar potential defined in the whole domain and in D_c , respectively. In Fig. (1), the wheelbases of the transistors (drain and source) (in blue), cables of the DC bus voltage (in green), capacitors (in yellow) and electrical load (in red) are taken into account. Each wheelbase corresponds to an electric port where the electric scalar potential v is constant. To optimize the discretization of the studied domain, the mesh of the PCB is based on a shell element method [3]. The 3-D mesh of studied domain consists of about 28.5k shell elements and 615k tetrahedral elements. Then, the CLN approach is performed to the FE model in order to derive an equivalent circuit of the PCB. In the case of a multi-inputs multi-outputs (MIMO) device with different ports [2], $\mathcal{M}$ branch currents $i_{0,j}$ with $j \in [1, \mathcal{M}]$ are introduced. To apply the CLN approach,

the FE model in the frequency domain using the Laplace transformation is written under the following form

$$\mathbf{K}\mathbf{X} + s\mathbf{N}\mathbf{X} = \sum_{j=1}^{\mathcal{M}} i_{0,j}(s)\mathbf{F}_j, \quad (1)$$

$$\forall j \in [1, \mathcal{M}] \quad Y_j(s) = s\mathbf{F}_j^T \mathbf{X} \quad (2)$$

with $\mathbf{X}$ the solution vector, $\mathbf{K}$ and $\mathbf{N}$ symmetric matrices depending on magnetic and electric behavior laws, $\mathbf{F}_j$ a source vector associated with the branch current $i_{0,j}(s)$ and $Y_j(s)$ for $j \in [1, \mathcal{M}]$, the quantities of interest. The MIMO case of the CLN approach is an extension of the single-input single-output self adjoint Lanczos algorithm. During the process of the CLN approach, two reduced bases of $\mathbf{A}$ and v are also defined in order to calculate an approximation of any field distribution. The coupling of the CLN equivalent circuit with the equations of the others components of the studied system is done naturally by considering the difference of the scalar potential v on the ports.

IV. NUMERICAL RESULTS

The equivalent CLN circuit of the PCB is composed of 12 stages which corresponds to 12 resistive and inductive matrices. The CLN circuit is combined with models of GaN transistors K_1 and K_2 . The GaN transistor model is based on the SPICE model of transistors GS66520B provided by the manufacturer [4]. To investigate the influence of the capacitors, two co-simulations are considered without and with capacitors C_1 and C_2 (see Fig. (1)). For both co-simulations, the time step is fixed to 0.1 ns and the simulation time is 7 μs (seven switching periods). The computational time of each co-simulation requires about 107 s (Intel Xeon 3.5GHz). Figures (2) and (3) present the waveforms of the current i_c associated with the load and the drain-source voltage V_{ds2} of K_2 . For

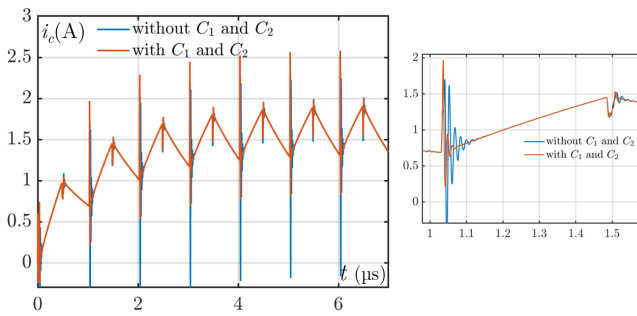


Fig. 2. Waveform of the current i_c obtained without and with the capacitors.

each waveform, the capacitors enable to reduce the ringing effect after each switching of K_1 and to significantly reduce the overvoltage of V_{ds2} which is 430 V and 255 V without and with capacitors, respectively. During the running of the co-simulation, the intermediate electrical quantities (currents and voltages) of the equivalent CLN circuit are stored. Then, these quantities and the reduced bases of $\mathbf{A}$ and v enable to calculate the distribution of the current density in the PCB layout for any time step. Figures (4) and (5) present the distribution of the current density for $t = 4.036 \mu\text{s}$ and $4.235 \mu\text{s}$ when K_1 is turn

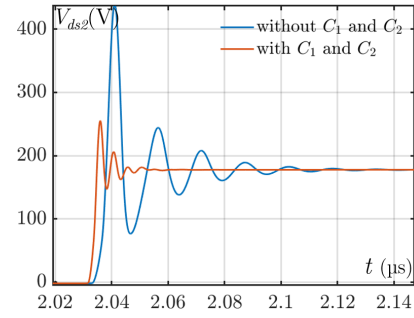


Fig. 3. Waveform of the voltage V_{ds2} obtained without and with the capacitors.

on. For $t = 4.036 \mu\text{s}$, the skin effect influences the distribution of current density. This time step is close to turn on of K_1 where high frequency oscillations of the load current i_c appear. For $t = 4.235 \mu\text{s}$, the distribution of current density is mainly influenced by the geometry of PCB layout. Additional results will be presented in the full version of the article.

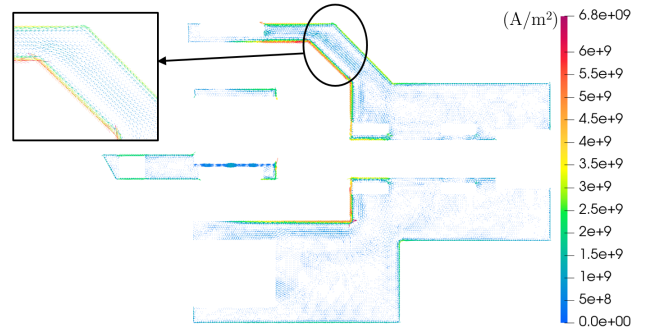


Fig. 4. Distribution of the current density for $t = 4.036 \mu\text{s}$.

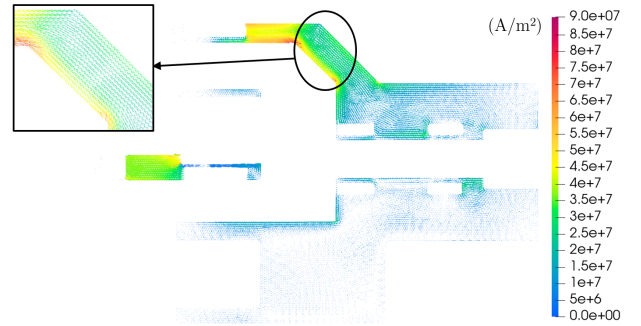


Fig. 5. Distribution of the current density for $t = 4.235 \mu\text{s}$.

REFERENCES

- [1] G. Antonini, A. E. Ruehli, D. Romano and F. Loreto, "The Partial Elements Equivalent Circuit Method: The State of the Art," *IEEE Transactions on Electromagnetic Compatibility*, vol. 65, no. 6, pp. 1695-1714, Dec. 2023.
- [2] T. Matsuo et al., "Multi-Port Model Order Reduction Using a Matrix Cauer Ladder Network," *IEEE Transactions on Magnetics*, vol. 56, no. 2, pp. 1-5, Feb. 2020.
- [3] H. Taha, T. Henneron, Z. Tang, Y. Le Menach, L. Pace and J. -P. Ducreux, "Electromagnetic Modeling of PCB Based on Darwin's Model Combined With Degenerated Prism Whitney Elements," *IEEE Transactions on Power Electronics*, vol. 38, no. 1, pp. 678-691, Jan. 2023.
- [4] <https://gansystems.com/gan-transistors/gs66502b/>