

A Study of Power-Hardware-In the-Loop based Motor Emulator for Inverter Open Circuit Faults

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A motor emulator is an active load that drains the desired current to flow through the inverter terminals. It uses the inverter phase voltage and the motor mathematical model to calculate the appropriate current reference value. In this paper, a power-hardware-in-the-loop (PHIL) simulation for motor emulation is proposed when the inverter gate drive failure occurs. In order to reconstruct the pulse width modulation (PWM) voltage into sinusoidal phase voltage, an integrator with a reset switch is used. When the inverter gate open fault occurs, the reconstructed voltage error causes current command divergence. The proposed method solves the problem of current command value diverging due to voltage reconstruction error. A control block diagram is proposed and its validity is demonstrated by the simulation.

Index Terms—Motor Emulator, Inverter Gate Open Fault, Power-Hardware-In the-Loop(PHIL).

I. INTRODUCTION

IN THE age of electric vehicles, the complete inspection of the inverter at the end of the production line is important. In the development stage, the inverter can be tested with the motor installed in the dynamometer system. However, the dynamometer does not fit the production line well due to the test time, cost, size, etc. Motor emulators that act like motors are widely used these days. It is an active load that allows the desired current to flow through the inverter terminal. It enables a realistic power testing of the drive inverter prior to machine prototyping. As a result, the launch time of the electric drive system has been greatly reduced [1]-[2]. The current command value of the inverter under test is obtained using the phase voltage and the permanent magnet synchronous motor (PMSM) model. To calculate the phase voltage, the PWM voltage in pulse form should be reconstructed to the phase voltage. It can be reconstructed to the phase voltage through an integrator consisting of hardware circuit [3]. In the event of a drive inverter failure, such as a gate-drive failure of one or more switches in the motor emulator system, the current has several harmonics. The motor emulator should emulate the current flowing due to drive inverter failure, and it is also important to be able to reliably emulate machine operation without damaging the system being tested under drive inverter failure conditions [4]. In this paper, a strategy for the motor emulation is proposed when the gate drive of inverter fails.

II. SYSTEM DESCRIPTION

A schematic of motor emulator system is shown in Fig. 1. Current drawn by the motor emulator system is equal to the current output by the motor model. To achieve the current command, driving inverter voltage $\mathbf{V}^I = [v_a^I, v_b^I, v_c^I]^T$. The PWM pulse voltage is reconstructed into a phase voltage by an integrator with reset switch as shown in Fig. 2. The motor model generates a current reference $\mathbf{I}^{I*} = [i_a^{I*}, i_b^{I*}, i_c^{I*}]^T$.

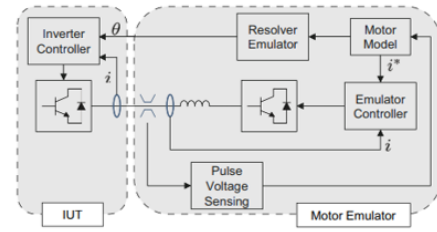


Fig. 1. Motor emulator architecture and implementation.

The motor emulator control is subsequently designed to ensure that the current drawn by the motor emulator equal to the current reference $\mathbf{I}^{I*}$. Fig. 3 shows the equivalent circuit of

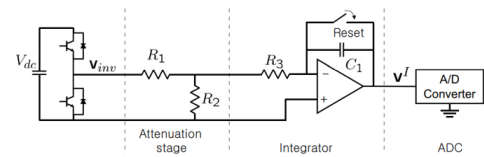


Fig. 2. Integrator with reset switch.

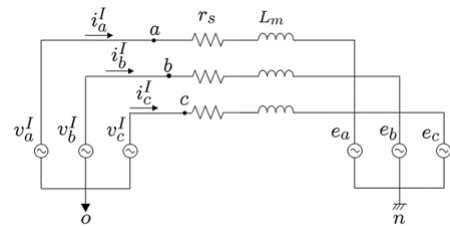


Fig. 3. Equivalent circuit of motor emulator.

the motor emulator. The input terminal of the motor emulator is defined as abc nodes. Note that, $\mathbf{V}^I$ is the voltage of abc nodes based on the inverter neutral point o , and the motor

voltage $\mathbf{V}^M = [v_a^M, v_b^M, v_c^M]^T$ is based on the motor neutral point n . By applying KVL to the equivalent circuit and solving the differential equation, the current command can be obtained.

$$\frac{d}{dt} \mathbf{I}^{I*} = -r_s \mathbf{L}_{abc}^{-1} \mathbf{I}^{I*} + \omega_e \mathbf{L}_{abc}^{-1} \psi_m + \mathbf{L}_{abc}^{-1} \mathbf{V}^M, \quad (1)$$

where r_s is the phase resistance, $\mathbf{L}_{abc}^{-1}$ is the inverse matrix of inductance, and ψ_m is back EMF constant respectively.

III. PROBLEM STATEMENT

Fig. 4. (a) shows the inverter voltage command, and Fig. 4. (b) shows the reconstructed inverter voltage when the a -phase gate driver upper switch open fault occurs at $t = 0.06$ s. If there is an error in the voltage measurement as shown in Fig. 4. (b), solving the differential equation will diverge the current command value.

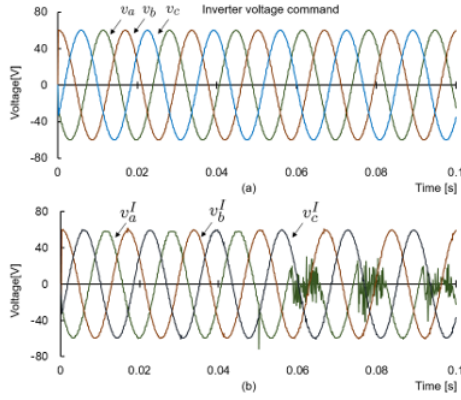


Fig. 4. Reconstructed voltage when the gate drive fault occurs at $t = 0.06$ s.

IV. PROPOSED METHOD

In order to prevent divergence of the current command value, the potential voltage between the neutral points is used. We can obtain below from the equivalent circuit.

$$\begin{aligned} \mathbf{V}^M &= [v_a - v_n, v_b - v_n, v_c - v_n]^T, \\ &= [v_a^I - v_{no}, v_b^I - v_{no}, v_c^I - v_{no}]^T. \end{aligned} \quad (2)$$

And applying KVL to the equivalent circuit, the following can be obtained.

$$\mathbf{V}^I - r_s \mathbf{I}^I - L_m \frac{d}{dt} \mathbf{I}^I - \mathbf{e}_{abc} = \mathbf{v}_{no}, \quad (3)$$

where $\mathbf{e}_{abc}$ is back emf, and $\mathbf{v}_{no} = [v_{no}, v_{no}, v_{no}]^T$ respectively. Considering that the sum of the three-phase current and back EMF is zero, then $v_{no} = (v_a^I + v_b^I + v_c^I) / 3$. The control block diagram of proposed method is shown in Fig. 5.

V. SIMULATION RESULTS

The simulation was performed using PSIM. For the same inverter controller, we compared the results with PMSM model and proposed motor emulator. Initially, 50% of the rated current was applied, and a -phase gate upper switch open fault occurred when $t = 0.025$. And 100% of the rated current was applied when $t = 0.06$. Fig. 6. (a) shows the current through the PMSM, Fig. 6. (b) shows the current through the motor emulator, and the two results are consistent.

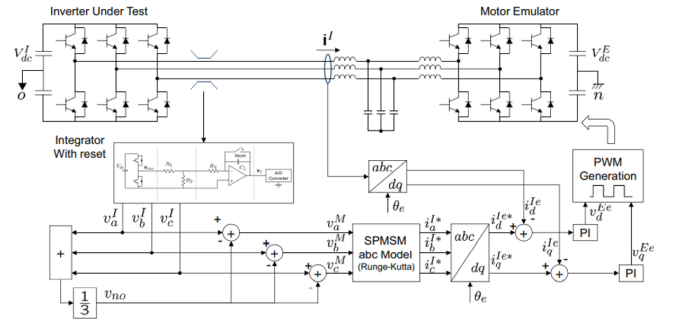


Fig. 5. Control block diagram of proposed method.

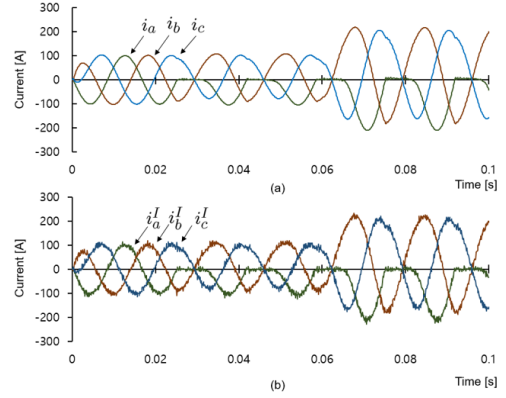


Fig. 6. Reconstructed voltage when the gate drive fault occurs at $t = 0.06$ s.

VI. CONCLUSION

More detailed descriptions, equations, and simulation results will be attached to the extended paper.

VII. ACKNOWLEDGMENTS

This research was supported by the Ministry of Trade, Industry and Energy (MOTIE) and Korea Planning & Evaluation Institute of Industrial Technology (KEIT) in 2025. (Project Number: 20024404)

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